CLAIMS

1. A parallel inverter system having a plurality of inverters, each of the plurality of said inverters comprising a synchronous unit for generating synchronous signals to ensure synchronization of a voltage given signals in the respective inverters which can be connected in parallel, a voltage given generator for generating a sine voltage with a given frequency, a phase and amplitude, a voltage regulating unit for regulating the inverter output voltage, and a power amplifier unit for converting directly a direct current power supply into an alternating current power supply, characterized in that each voltage regulating unit of each inverter includes a voltage regulator circuit and a voltage linear combination circuit, and the voltage linear combination circuit combines linearly all of the output voltages of the voltage regulator, and then outputs them to the power amplifier unit.

2. The parallel inverter system of claim 1, characterized in that the synchronous unit is a synchronizing square wave generator, wherein precise high frequency oscillating signals are generated by an oscillator in the synchronizing square wave generator, output to the divider to form a square wave with the power frequency, and then output though an OC gate and fault shield switch K2, and then output the outputs of respective dividers after AND to the voltage given generator as synchronizing square waves.

3. The parallel inverter system of claim 1, characterized in that in the voltage given generator a voltage virtual value given circuit inputs a required voltage virtual value, which is outputted to a sine wave generator through a virtual value regulating circuit; a phase discriminator receives the synchronizing square wave output by the synchronizing square wave generator, and constitutes a phase-locked loop with the sine wave generator; the output terminal of the sine wave generator connects the voltage regulating unit, and the output impedance circuit can linearly combine the outputs of the various sine wave generators through the impedance circuit and the fault shield switch (K3) to give it as the voltage of the voltage regulating unit.

4. The parallel inverter system of claim 1, characterized in that the amplifier unit includes a SPWM generator, a driving circuit, a power switching tube and a filter

connected in turn; the high frequency SPWM waves generated by the SPWM generators are used to drive power switching tubes after they are amplified by the driving circuit, the power switching tubes are turned on and off alternately to convert the direct current into amplified SPWM wave, and the amplified SPWM wave is moved the carrier wave by the filter to get the amplified sine alternating-current power supply.

5. The parallel inverter system of claim 1, characterized in that in the voltage regulating unit the voltage regulator can be P regulation, PI regulation or PID regulation; and a voltage linear combination circuit comprises an output impedance and a fault shield switch (K4).

6. The parallel inverter system of claim 1, characterized in that the voltage regulator unit can also include a saturation suppression circuit, the saturation suppression circuit detecting the difference between the output voltage of the voltage regulator and the output linear combination value of the parallel inverter system, and feeding back to it to the voltage regulator.

7. The parallel inverter system of any one of claim 1~6, characterized in that the current regulator unit for regulating the distortion of the inverter output voltage and realizing the even distribution of the load of respective inverters is connected between the voltage unit for regulating the power amplifier unit of the present invention.

8. The parallel inverter system of any one of claim 1~6, characterized in that the following relation exists between the output voltage of respective voltage regulator *V_PI(j)* and the output voltage of the voltage linear combination circuit after linear combination *V_PI_out*, $V\_PI\_out = \sum_{j=1}^{N} K(j) \cdot V\_PI(j)$, wherein *K(j)* is weight number, $\sum_{j=1}^{N} K(j) = 1$.

9. The parallel inverter system of any one of claim 1~6, characterized in that the following relation exists between the output voltage of respective voltage regulator *V_PI(j)* and the output voltage of the voltage linear combination circuit after average

V_PI_out, $V\_PI\_out = \sum_{j=1}^{N} V\_PI(j) \div N$, wherein N is the number of the parallel inverters.